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U.S. UTILITY Patent Application

PATENT NUMBER and  
ISSUE DATE

APPL NUM 10079472	FILING DATE 02/19/2002	CLASS 257	SUBCLASS	GAU 2314	EXAMINER
APPLICANTS: Mahajan, Maitreyee; Walker, Andrew; Kouznetsov, Igor,					
<p>**CONTINUING DATA VERIFIED: <i>NC</i></p> <p>**FOREIGN APPLICATIONS VERIFIED: <i>no</i></p>					
PG-PUB DO NOT PUBLISH <input type="checkbox"/>			RESCIND <input type="checkbox"/>		
Foreign priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no			ATTORNEY DOCKET NO.		
35 USC 119 condition met <input type="checkbox"/> yes <input checked="" type="checkbox"/> no			40025-005		
Verified and Acknowledged Examiner's initials					
TITLE : Gate dielectric structures for integrated circuits and methods for making and using such gate dielectric structures					

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NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
Assistant Examiner		DRAWING	
ISSUE FEE		Sheets Drwg.	Figs. Drwg.
Amount Due	Date Paid	Print Fig.	
Primary Examiner		Application Examiner	
<input type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368, Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.	

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